RFRD
Radio Frequency Readout Device

DESIGN DOCUMENT FINAL

Team: 18

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Contents

1 Introduction

1.1 PROJECT STATEMENT

The goal of this project is to develop an RF sensor system that can read a capacitance value from a passive tag from at least five meters away. In an acronym, the goal of our project is to develop a Radio Frequency Readout Device (RFRD); we will be using a capacitance sensor for the first sensor build.

1.2 PURPOSE

This project, in just the application for which we designed it, allows us to take a capacitance measurement from a distance. For two metal plates of constant material between them, a capacitance measurement is essentially a distance measurement - so anywhere this tag is implanted would let us gauge the distance between two metal plates - potentially useful for nondestructive evaluation of any construction. The specific application will be connecting an RF tag to each of the bolts on a street-side light post that will include eight capacitance sensors each that can be used to determine whether the bolts are tight or loose.

Going past merely measuring capacitances, this tag will let us transmit information given any transducer capable of generating a series of digital voltages to correspond to a value.

1.3 GOALS

Our main goal is to measure capacitance from at least five meters using an IC prototype that will harvest RF energy from a reader to power a capacitance sensor and transmit said data back to the reader. The reader will subsequently transmit this data to either a smartphone or a computer, which will upload the data to the cloud when available. More specific goals for our project are included in the list below:

1.3.1 GOALS ACCOMPLISHED

- Successfully program an Arduino Mega 2560 Microcontroller to create a 13.56 MHz signal. Power output was too low, need to redesign the circuit.
- Successfully transmit a 13.56 MHz signal across two (square coil) antennas
- Conduct performance tests for our capacitive sensor design on Cadence
- Build a breadboarded IC prototype of our multiplexor logic circuit and corresponding power rectifier, 13.56 MHz clock counter

1.3.2 GOALS FOR NEXT SEMESTER

- Build data modulator for our breadboarded IC prototype that can operate with a 13.56 MHz signal.
- Build a breadboarded prototype of our capacitive sensor
- Transmit modulated data from our logic circuit prototype over across two antennas

- Model appropriate demodulator for demodulating incoming data from the IC prior to sending it to the Microcontroller
- Work on an Analog to Digital converter that converts the incoming analog data before sending it to the Microcontroller
- Address any design issues encountered during prototyping phase
- Develop Demodulator and Analog to Digital Converter on reader end
- Determine how we will differentiate multiple tags- either through inclusion of embedded nonvolatile memory or distinct time delays for tags in close proximity (i.e. for each of the tags corresponding to the bolts of a single light post)
- Integrate the components on the tag side into an integrated circuit design
- Finalize the capacitive sensor design
- Integrate each of the three subsystems of our design (including the RFRD Reader, the RFRD Tag, and the antennas for interaction between the reader and tag)
- Be able to successfully obtain the capacitance data from five meters using an IC that will harvest energy from a reader to power a capacitance sensor and transmit said data back to the reader
- Develop a user interface for accessing the data from the Microcontroller and displaying it in an orderly and user friendly fashion

2 Deliverables

The goal of the first semester is to have a functional lab-ready prototype device that serves as a proof of concept for each of the subsystems in the project as well as the overall system. By semester's end, we intend to have:

- A prototype, custom circuit capable of transmitting static data
- A prototype reader that is capable of sending a 13.56 MHz power signal across two antennas.
- A website containing information and documents regarding our project

By the end of the project next semester, we intend to have:

- A batteryless system capable of receiving and sending a signal, consisting of:
    - A prototype RFID circuit capable of transmitting capacitance data
    - A reader that is able to receive tag data and transmit received data to an external source
    - Software capable of storing captured data both locally and in the cloud

3 Design

3.1 SYSTEM SPECIFICATIONS

3.1.1 Non-functional

- IC
    - The RFRD tag must cost less than 50¢.
    - The tag size should be limited to the scale of millimeters, but is less crucial than cost considerations.
- Reader
    - The size of the reader is inconsequential.
    - The reader does not need to be battery-powered.
    - The cost of the reader is negligible compared to the cost of the tag.
- Antenna
    - Transmitting antenna should be a manageable size (should not need to be carted around, for example)
    - Receiving antenna should be appropriately durable and small enough to fit in its application.

3.1.2 Functional

- IC
    - The tag needs to be passive. It must harvest all of its power from the incoming signal from the reader.
    - Tags must include an antenna for signal reception/transmission.
    - Tags must include identification data in the form of nonvolatile memory that can be utilized to uniquely differentiate the tags for each of the bolts on a light post (or a similar method of identification, such as programmed clock delay).
    - Capacitance sensors need to be able to determine whether the bolt is 'tight' or 'loose' (will readout a '0' for tight or a '1' for loose).
- Reader
    - The RFRD reader must be able to successfully retrieve capacitance data, from the RFRD tag at a minimum distance of 5 meters.
    - The reader should transmit and receive a signal with carrier frequency of 13.56 MHz for the purpose of testing and possibly 900 MHz for the final product in which the capacitance and identification data for each tag will be embedded.
    - The reader must be able to receive the incoming signal from each tag, capture the corresponding capacitance data, and identify which tags are linked with loose/tight bolts.
- Antenna
    - Receiving antenna must capture enough power to be able to drive every subsystem of the tag. This may require the transmitting antenna to be

able to handle an especially large input power, given the 5 m target distance of the application.

3.2 PROPOSED DESIGN/METHOD

For the tag part of the project, we have designed our capacitance readout to be run into a bit string via cascaded multiplexers (though we are now considering the use of 8-bit registers for the purpose of prototyping). The bit string is divided into four sections: start, ID, sensor data, and end. The multiplexer will step through the bit string and send the bits to the modulator, cycling through repeatedly while powered. The sensor circuit will consist of an array of capacitors, which will be charged, read into the multiplexor, and discharged before repeating the cycle.

For the reader portion of the project, we have undergone several design and method changes as the requirements of the project have been better defined and as we've learned more about the limitations of the methods that we had previously chosen. Initially, we were planning to use the 900 MHz band RF radio paired with a Raspberry Pi 3 to store and transmit the data between a smartphone or other data source. However, as we did more research into that particular radio band, we discovered that the radios that would support it, as well as the SDKs for the devices, are very costly and the documentation available is very limited, which doesn't tell us if the radios could do what we need them to.

After some deliberation, we decided to switch to using the 13.56MHz band for communication. This band has cheaper, more readily available parts to work with and will allow us to test things with the test equipment we have access to. Unfortunately, most radios available for this band have very low range, normally less than 1 meter. This is because most 13.56 MHz radios use near field communication technology. Due to this, instead of purchasing an antenna, we have decided to build the antenna for our reader, which will give us more flexibility in how we transmit power and receive signals. We also hope it will be cheaper to work with. We are still deciding how the reader will interface with a computer/smartphone and send data to the cloud.

Work on the antenna has depended on the decision to reduce the operating frequency from 900 MHz to 13.56 MHz. The decision to reduce the frequency has significantly increased the rate of development, as it allows us to perform testing with readily available function generators.

The rectifier circuit, in turn, depends on the antenna. This is because the input impedance, and thus the antenna-rectifier impedance match, depends on the input power that comes in from the antenna. Once an antenna with suitable gain has been derived, then, an estimation for received power can be calculated and a suitable rectifier circuit can be modeled and calculated.

3.3 DESIGN ANALYSIS

For the reader portion of the project, we recently received parts and have begun working on the initial design. We have successfully been able to send out a 13.56 MHz signal from the reader, but have not been able to receive data back from a tag yet. We are working on receiving a signal from the RFID tag we have for testing, and demodulating the data it gives us. Once we have our reader working with the test RFID, we will begin working to see if we're able to read the prototype the IC team is working on.

For the tag team, we have prototyped and tested some power harvesting circuitry to see how much power the system could harvest at various input levels. Our initial test showed that we were unable to drive the circuitry with a typical input voltage. As a result, we began looking into some lower threshold voltage diodes as an option to replace our standard ones in our discrete prototype. For our logic design, we originally thought of having a long string of D flip flops to pass the data to the antenna; however, this idea would have had a lot of dynamic power usage and taken a lot of area. We then decided to switch to a giant (64 bit) multiplexer for our logic. The advantages of this design is that we save area by eliminating the DFFs in the start and end signals by tying them to VDD and ground. We also save power because we eliminated the DFF which means less transistors transitioning between high and low states.

We ordered a number of 8 bit multiplexers in order to model a 64 bit multiplexer for the purpose of testing on a breadboard. However, we are now considering the possibility of using two 8-bit registers and one 2-bit multiplexer instead for the purpose of prototyping. This would require testing with only four incoming capacitance readings rather than the eight we would like to have on each tag, but it is also easier to work with the 8-bit registers for the purpose of prototyping and should be able to do the same thing. We have also conducted initial prototyping for the capacitance sensor circuit. However, in this case we ran into trouble with the fact that the MOSFETs we have experience a lot of leakage power. We have since ordered new MOSFETs that we will hopefully be able to work with.

For the antenna team, as stated above, the decreased operating frequency has significantly stimulated the development of the project. The trade-off with a lower operating frequency is a longer wavelength (which increases functional distance) in exchange for a lower antenna efficiency (which decreases functional distance). Empirical breadboard tests show that a square coil wire antenna geometry offers significant radiative and logistical (e.g., space, mechanical implementation) advantages. With the information gained from this testing, a parameterized and easily-modifiable square coil antenna was constructed in HFSS and tuned for maximal gain.

In the rectifier, a harmonic balance simulation is performed to account for the nonlinearities in the diode's I-V characteristic. Using this simulation, an understanding could be developed as to the dependence of dc output voltage and current on input power and source impedance. Thus, a source impedance match can be calculated.

4 Testing/Development

4.1 INTERFACE SPECIFICATIONS

The hardware from the IC tag will communicate via RF signals with a reader. The reader will interpret the RF signals and display something to the user to convey whether the washer is tight or loose. The layout and design of the project are pretty open ended.

4.2 HARDWARE/SOFTWARE

The block diagram schematics for the RFRD Reader and Tag are included in the appendix as fig. 1 and fig. 2, respectively. We are using two different methods to test and design our circuit. The first method is prototyping on a breadboard using discrete components. Our primary goal for this semester is to get the breadboard or perfboard design tested and functioning as expected. This allows us to make sure that the logic and design concepts are working as expected. It also allows us to test our antennas to see how much power output can be transmitted at different distances. However, it will not be representative of the power consumption of our final IC design.

The other method that we are using is Cadence to simulate the various components. Using Cadence allows us to see a more precise value for the power consumption that the circuit will use. It also helps us to determine the area that the IC will consume. Most of the testing in Cadence has been performed for the capacitance sensor. Further information and schematics are available in the appendix under figs. 3.

For the antenna and rectifier, hardware includes solely the antenna and the rectifier circuit. The only relevance of software is for our own faster simulation, testing, and calculation.

4.3 PROCESS

For the reader team, our original idea was to buy a programmable module. However, the module was $700, and we decided to work at the cheaper 13.56 MHz frequency instead of testing at the more expensive frequency range. This led us to search for modules at the new frequency range; however, most of them could only work at very small distances. Therefore, we decided to design our own module based off of a collection of various chips.

For the tag team, we started with building a standard full bridge rectifier and DC - DC boost circuit to be able to operate an IC and sensor. We also built an initial modulator circuit to send data back to the reader. The next step was to design an IC capable of measuring capacitance and sending data bits to the modulator. We are working with the antenna team to collect power from the reader via RF, and power the IC with the boost circuit. We are also working with the reader team to develop an IC which will send readable data to their reader.

On the antenna team, testing started with two breadboards sitting face to face, each with an infinitesimal dipole. We drove the first antenna with a function generator and measured the voltage on the second. From here we experimented further with the geometry and extra circuitry. We found that a square coil antenna performed significantly better than other geometries.

Once we knew the optimal high-level antenna geometry, the next task was rectification. We found the PSPICE model for the Avago HSMS2822 diode, mentioned in an RF energy harvesting paper, and implemented a half-wave rectifier test circuit in ADS. We then simulated this circuit with harmonic balance and a power source to model the antenna itself. The antenna-rectifier impedance match depends on the power incident to the antenna, so from here the next step is to model and tune a square coil antenna. This was done in HFSS.

5 Results

IC Team:

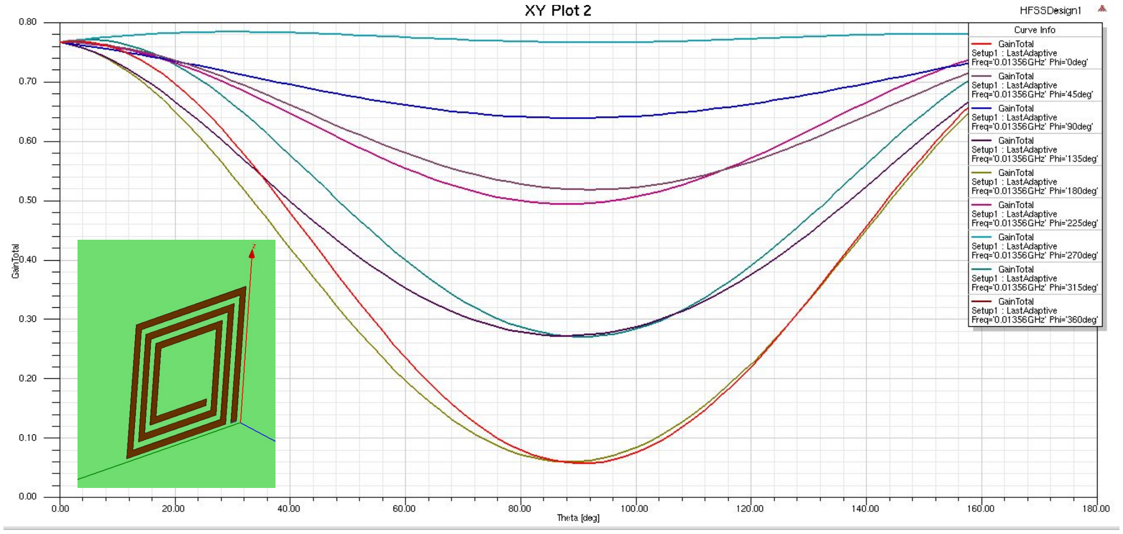
We have a breadboard prototype of the tag IC (see Image 1 in Appendix), without the rectifier or clock circuitry. We are testing the components in this design with a dc power supply, and square wave input. Thus far, the counter and logic for charging/discharging the capacitor is working, but the charging/discharging circuit, and the data output are not fully working. The charging circuit is working in simulation, however.

Antenna Team (Mehdy):

(Mehdy, 11/3) On the task of working with the antennas, I found a ~350 mV_{pp} amplitude on the receiving end when I had a function generator connected to a small dipole. This was with the transmitting and receiving antennas ~1 cm apart from each other. I think this dismal result is the result of lack of impedance matching components plus usage of short antennas. Success in testing then, for me, depends on usage of matching networks and longer antennas. I can also use HFSS to simulate the antennas I design so that I get an accurate calculation of their impedance - using that input impedance I can design the matching network I want to transform that impedance. My first move from here is going to be breadboarding a wide variety of longer antennas, possibly in arrays, to experiment with their effectiveness.

(Mehdy, 11/6) While working with the antennas further, I found that increasing antenna length increased received voltage amplitude by about 10%. I then soldered some of my kit's long wires together and bent the geometry into a square spiral shape for both the transmitting and receiving antennas. This gave me a 2.28 V_{pp} signal at the receiver with 10 V_{pp} input into the transmitter - a very encouraging improvement, over six times the received amplitude with 10 V_{pp} into the single infinitesimal dipole antenna.

(Mehdy, 12/1) I simulated a square coil antenna in HFSS, tuning its geometry for optimal gain. I found that ignoring loss due to mismatch, the gain of this antenna is about 0.76. By the Friis transmission equation, at 5 m, this allows for an optimistic $P_{received}$ / $P_{transmitted}$ ratio of 0.071514. In the below plot for this antenna's gain, the curve of most interest is the cyan curve, which represents the gain vs. theta for phi equal to 270 degrees: the axis which goes through the center of the square coil.



6 Conclusions

On the antenna and rectification task, we have an antenna which stands to be able to receive milliwatts at 5 m. We also have a working simulation environment for the rectifier, and a fast method of deriving via ADS the impedance match between the antenna and rectifier circuit given the diode's power-dependent input impedance.

On the reader team, we have obtained the first set of parts for our reader and we are working to get the prototype reader assembled. At this point we have a reader generating the 13.56 MHz wave to power the tag. We find it necessary to build a reader from scratch for two reasons. One, most of the 13.56 MHz RFID modules that we could find had internal antennas, mostly using near field communication, which does not work for this project. Second, we want to be able to be able to quickly change the frequency we are using if we find 13.56 MHz does not work.

On the tag team, we are working with the antenna team to get power through to our IC circuit. Our main goal, however, is building the IC circuit to test the measuring capabilities. At this point, we have some promising results from simulation testing of the sensor circuit in Cadence. We have also performed some successful tests with the discrete components we are using to model the integrated circuit. Moving forward we will want to complete further prototyping including the integration of all the necessary parts for modeling the tag. From there we will begin work on the design of the integrated circuit for the final product.

7 Project Research Sources

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8 Appendices

RFRD Reader Block Diagram:

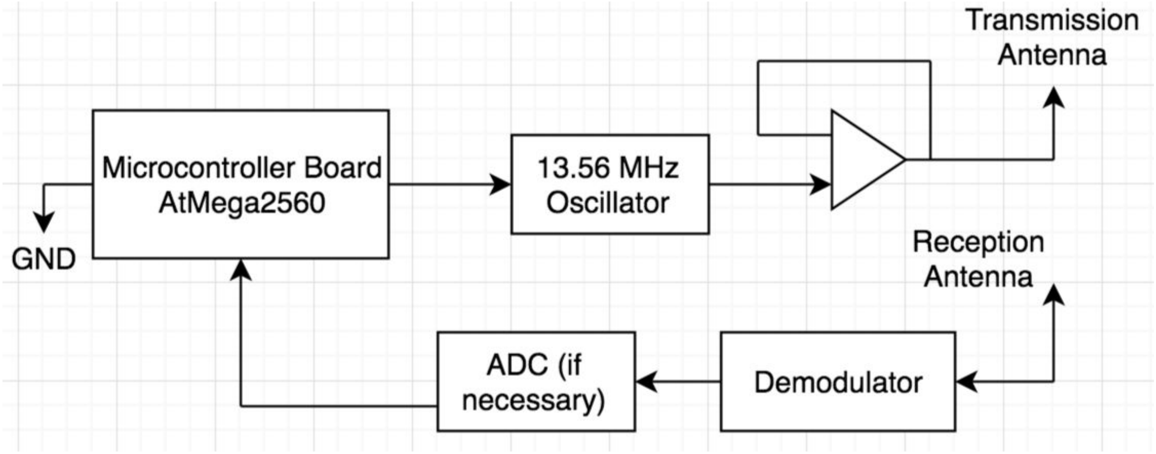

fig. 1

The above image shows our current design concept for our reader. Right now we are planning on using an Arduino to power an oscillator to send a 13.56 MHz signal as shown above. We placed a buffer between the oscillator and the antenna to prevent any possible noise from the tag side. We are then going to read the tag signal through a separate antenna, demodulating the signal, and sending that either to a discrete ADC or the ADC built into the Arduino.

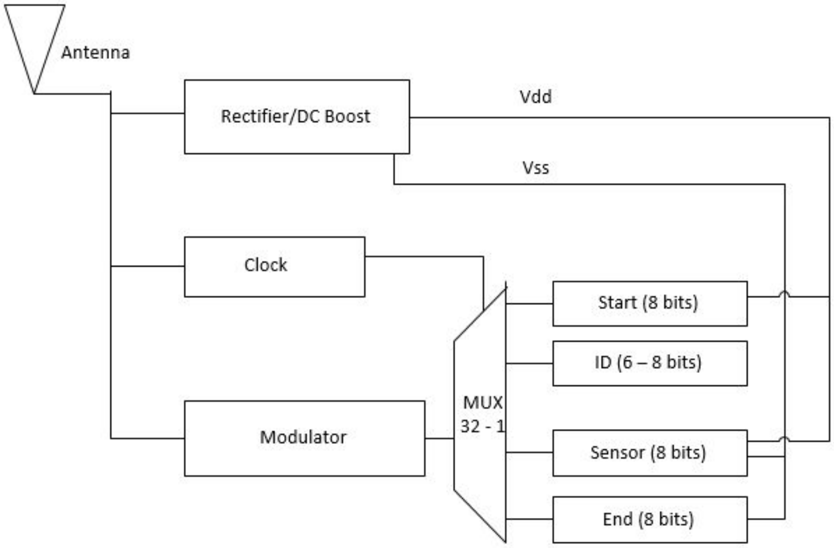

fig 2.

The diagram above outlines the basics of our tag, with a single antenna, power harvest, sensing, and data transmission. The clock section will reduce the antenna signal at 13.56 MHz to 1.695 MHz. The start bits are tied to Vdd to help provide a baseline high level, as are the end bits, which provide a baseline low voltage level.

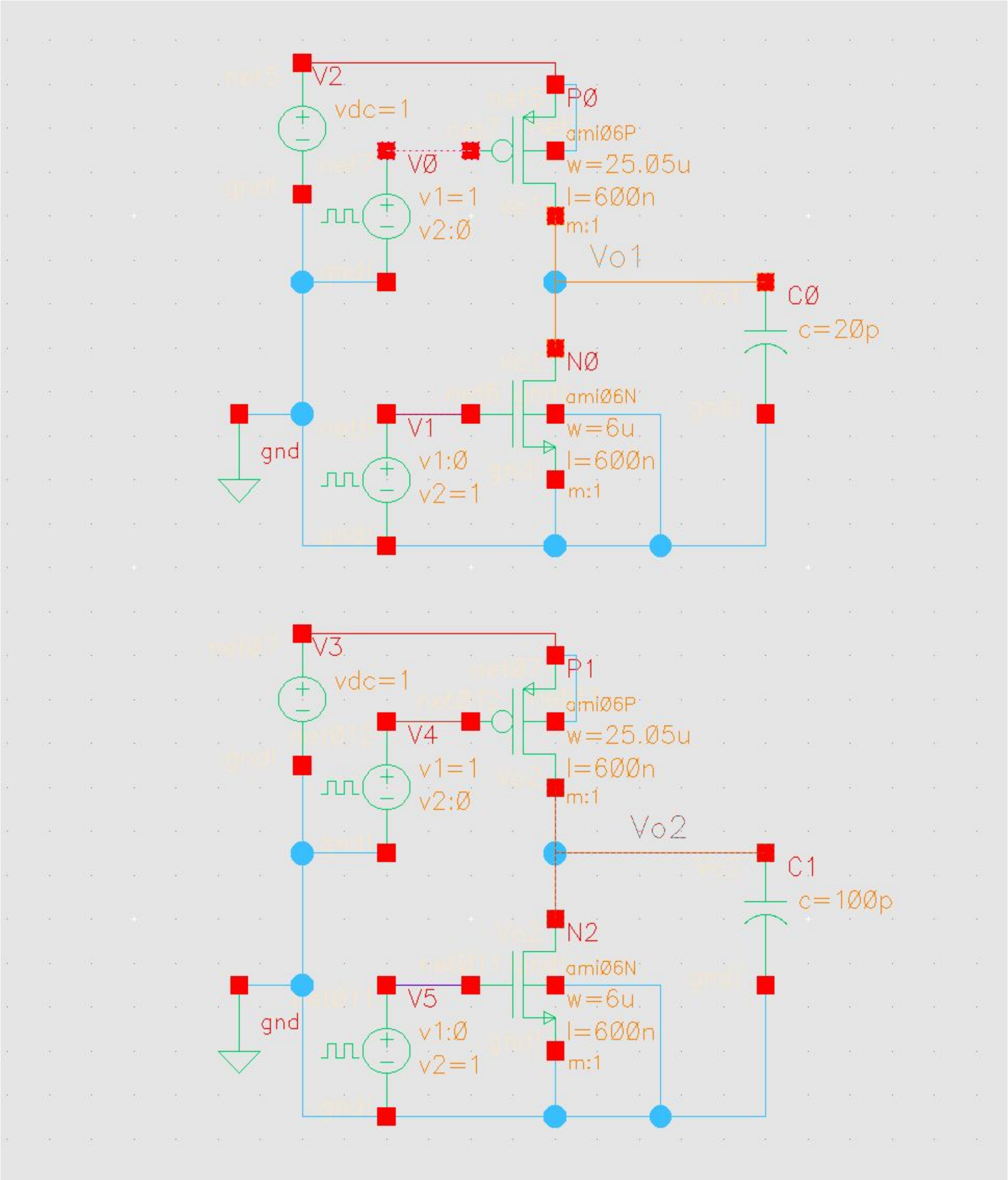

fig. 3

This image outlines the basics of our capacitance sensor, which is on the far right. The V0 pulse simulates a single bit of the start bit section, which turns on the N1 NMOS to charge the capacitor for a short amount of time. The lower N0 NMOS device grounds out the capacitor during the end bits to reset its value to Vss before it is recharged during the start bits.

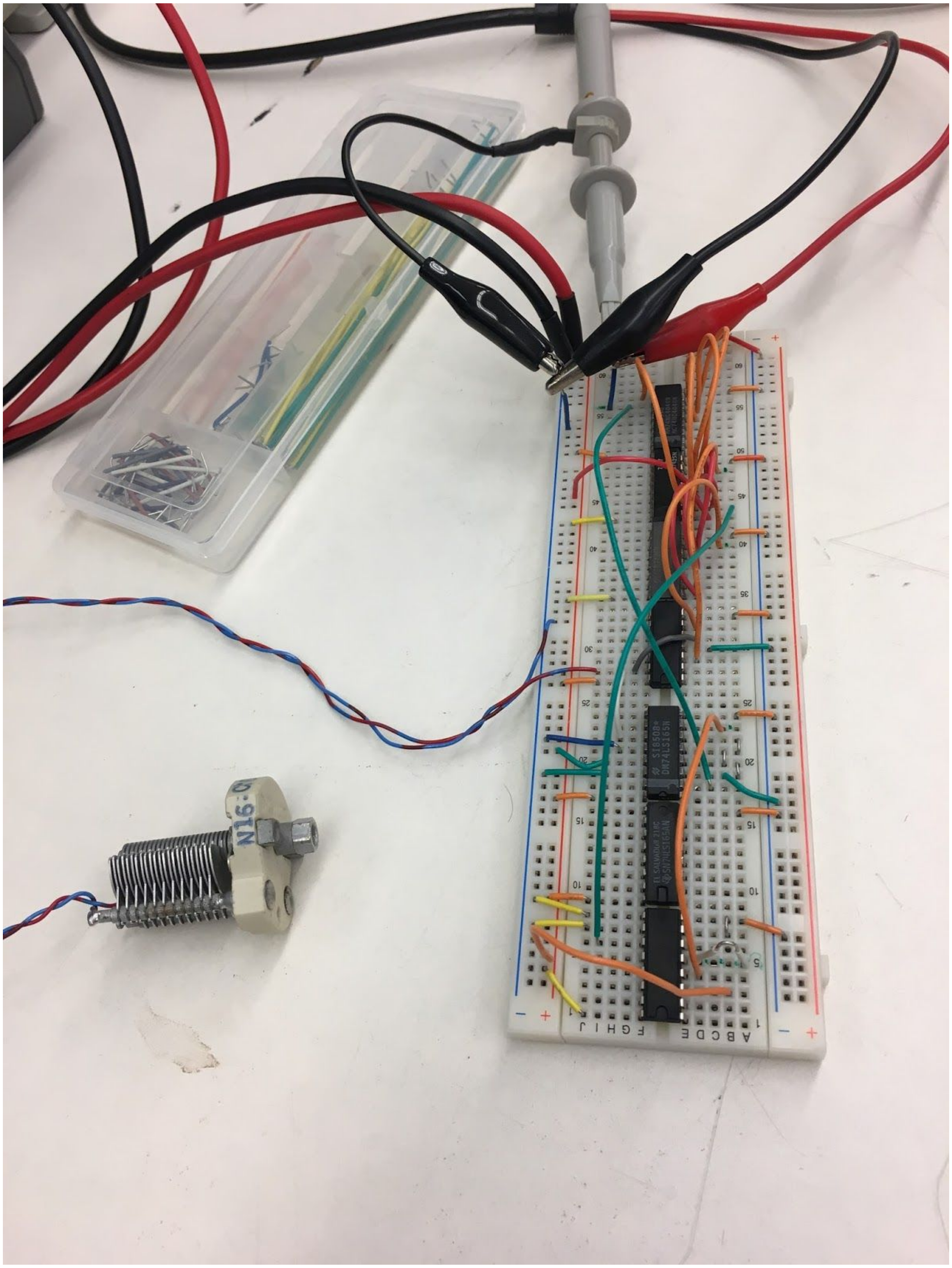

Image 1: Breadboard prototype of IC tag without DC rectifier or antenna to clock.