EE 492 WEEKLY REPORT 16 *Date: 2/7/17-2/13/17*

Group number: 18

Project title: Radio Frequency Readout Device (RFRD)

Client &/Advisor: Dr. Qiao

Team Members/Role: Brandon Baxter/Team Leader, Vaughn Dorsey/Team Webmaster, Luke Myers/Team Communication Leader, Kurt Turner/Team Key Concept Holder, Aaron Haywood, Robert Buckley, Mehdy Faik, Kellen Yoder, Michael Miller

- **Weekly Summary**

This week we began work on the PCB prototype design including looking into necessary parts. Also further simulation work was performed as well as design work in Cadence.

- **Past week accomplishments**
  - Brandon Baxter: Planned and reviewed parts necessary for the PCB prototype
  - Vaughn Dorsey: Continued work on developing the reader companion software.
  - Luke Myers: I discussed prototype situation with Kurt.
  - Kurt Turner: Worked on Cadence simulation of IC Tag. Worked on Prototype PCB.
  - Aaron Haywood: Tested amplifier and filter for reader
  - Robert Buckley: Worked on simulation of the shift register and counter to determine power needed to run the circuit. I have started looking into how to simulate the power needed for the internal IC, cap censor, and demodulator through pad frames.
  - Mehdy Faik: Learned Eagle. Laid out rectifier board in full. Sent exported gerber files to Lee. Edited gerber files to make them workable for him. Should be good.
  - Kellen Yoder: Worked on PCB MultiSim design, also started to think about the poster aspect of the project.
  - Michael Miller:
- **Pending issues**
  - Brandon Baxter: Worked on…
  - Vaughn Dorsey: None at this time.
  - Luke Myers:
  - Kurt Turner: Noise, still.
  - Aaron Haywood: Amplifier still has issues. Possibly frequency related.
  - Robert Buckley: Encounter is not working so layout is difficult. We can make it by hand if necessary...

- Mehdy Faik: Lee hasn't emailed me back. Wasn't in his office the time I went down to check on him, about Wednesday ~4pm.
- Kellen Yoder:
- Michael Miller:

o Individual contributions

NAME	Individual Contributions	Hours this week	HOURS cumulative
Brandon Baxter	Meeting with Advisor and PCB preparation	3	12
Vaughn Dorsey	Software Development & Meetings	3	14.5
Luke Myers	Demodulator work. Discussed prototype.	3	15.5
Kurt Turner	Cadence simulation Prototype layout	4.5	17.5
Aaron Haywood	Amplifier and filter build/test	3	13
Robert Buckley	Simulating power requirement of IC.	5.5	27.5
Mehdy Faik	Learned Eagle. Laid out rectifier board in full. Sent exported gerber files to Lee.	8	34.25
Kellen Yoder	Meeting w/ Advisor, PCB stuff, Poster ideas	3	14
Michael Miller			

o Plan for coming week

- Brandon Baxter: PCB design hopefully to be completed this next week.
- Vaughn Dorsey: Continue Software Development with focus on creating database schema.
- Luke Myers: Begin work on the design document.
- Kurt Turner: Assist with PCB design. Insert Cap sensor into Cadence simulation.
- Aaron Haywood: Continue debugging the amplifier
- Robert Buckley:
- Mehdy Faik: Antenna machining. First priority is getting in contact with whoever's going to actually cut it, because I don't know otherwise what they want to be able to do that job.
- Kellen Yoder: Finish PCB in Multisim, help out with any IC or Reader activities that need assistance
- Michael Miller:

o Summary of weekly advisor meeting

Eight members present in addition to Dr. Qiao and Dr. Song

Vaughn discussed what he currently has developed for the user interface, which will be talking directly the the arduino. Dr. Qiao wanted to know more about what will be present on the reader. We may need to develop a second pcb specifically to support the reader end in addition to that for the IC tag.

We spoke about initial work for the printed circuit board and going from through hole to surface mount. We are currently looking into chip options for moving from the prototype for the actual printed circuit board itself. We need to find the pin sizes prior to beginning development of the actual pcb design itself. Stand alone capacitance sensor was $1 per chip. We need to do more research on capacitance sensor options. TI Capacitance chip will require higher cost with supply voltages at minimum 3 voltages.

At the moment, the power consumption right now is between 2 and 4 mw with the discrete components. Michael and Robert have developed most of the IC design in Cadence.

We discussed power consumption possibilities on the IC side. We discussed what we can do to successfully implement some testing on our current design as soon as possible. We need to do testing prior to building the design of our pcb itself.